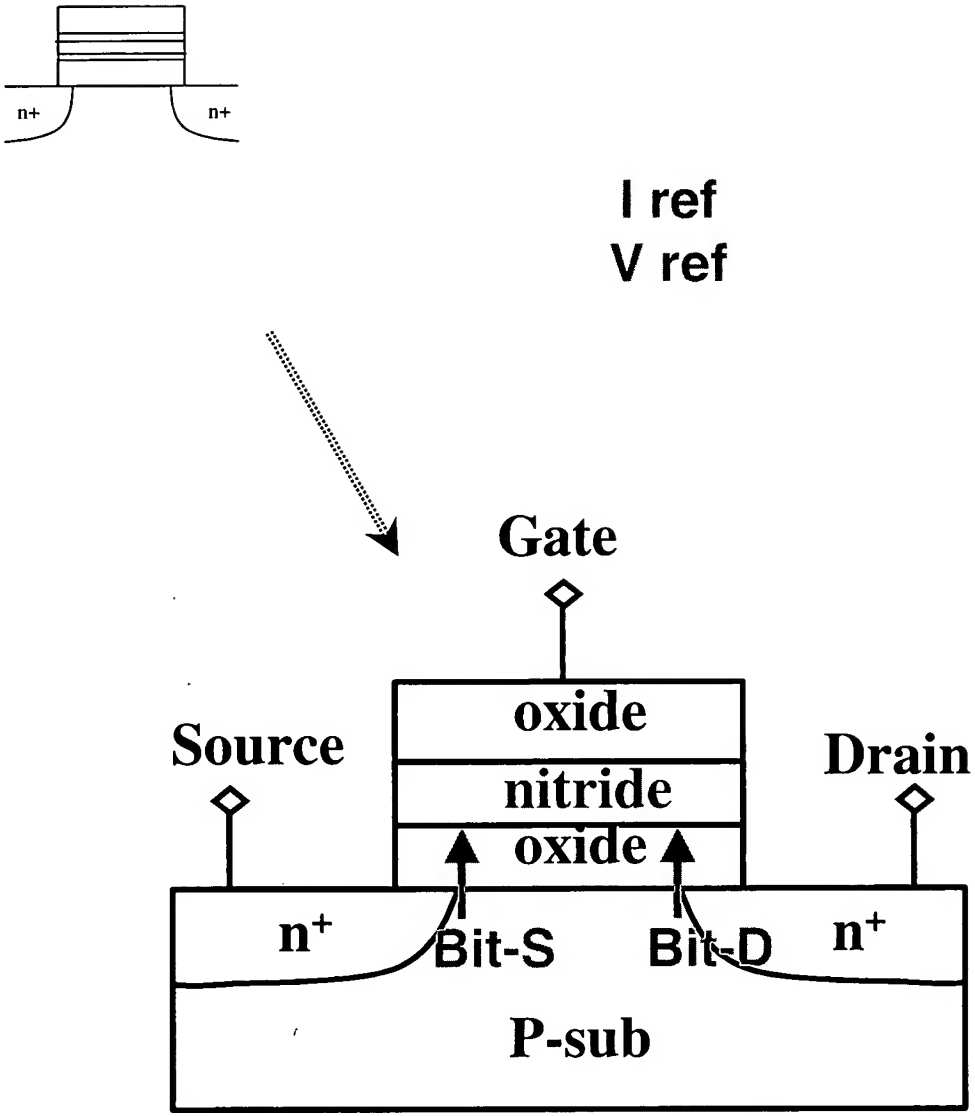
Fig. 1


n+
n+
I ref
V ref
Gate
Source
oxide
nitride
oxide
Drain
n+
Bit-S
Bit-D
n+
P-sub

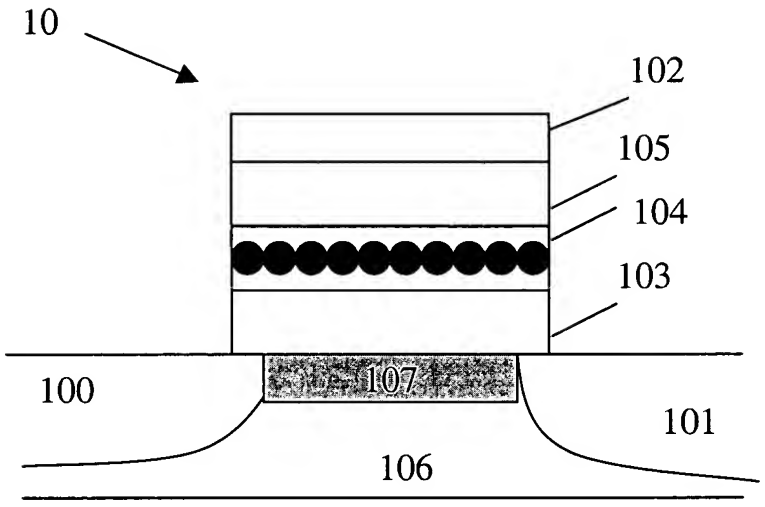

10
102
105
104
103
100
107
101
106

Fig. 2

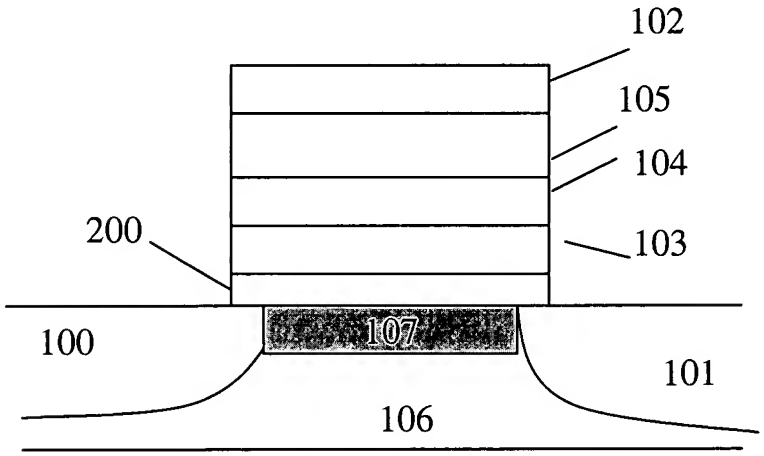

102
105
104
200
103
100
107
101
106

Fig. 3

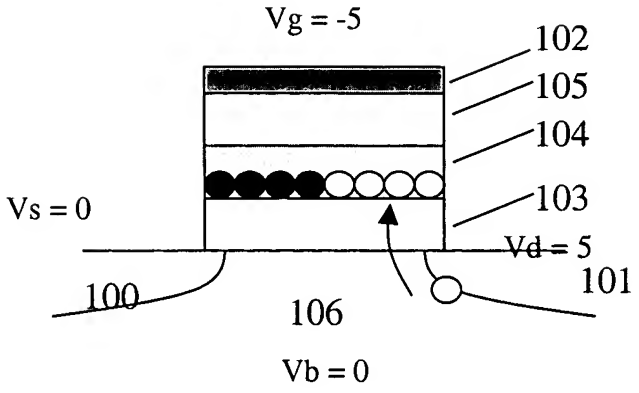

Vg = -5
102
105
104
103
Vs = 0
Vd = 5
100
101
106
Vb = 0

Fig. 4A

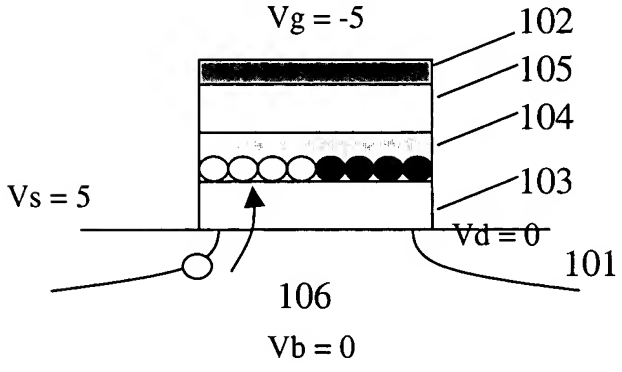

Vg = -5
102
105
104
103
Vs = 5
Vd = 0
101
106
Vb = 0

Fig. 4B

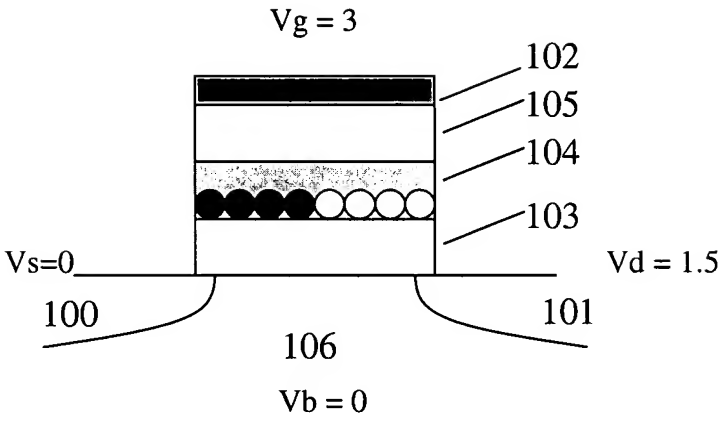

Vg = 3
102
105
104
103
Vs=0
Vd = 1.5
100
101
106
Vb = 0

Fig. 5A

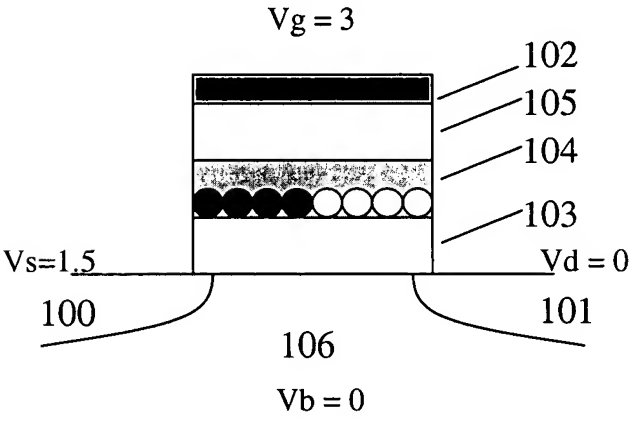

Vg = 3
102
105
104
103
Vs=1.5
Vd = 0
100
101
106
Vb = 0

Fig. 5B

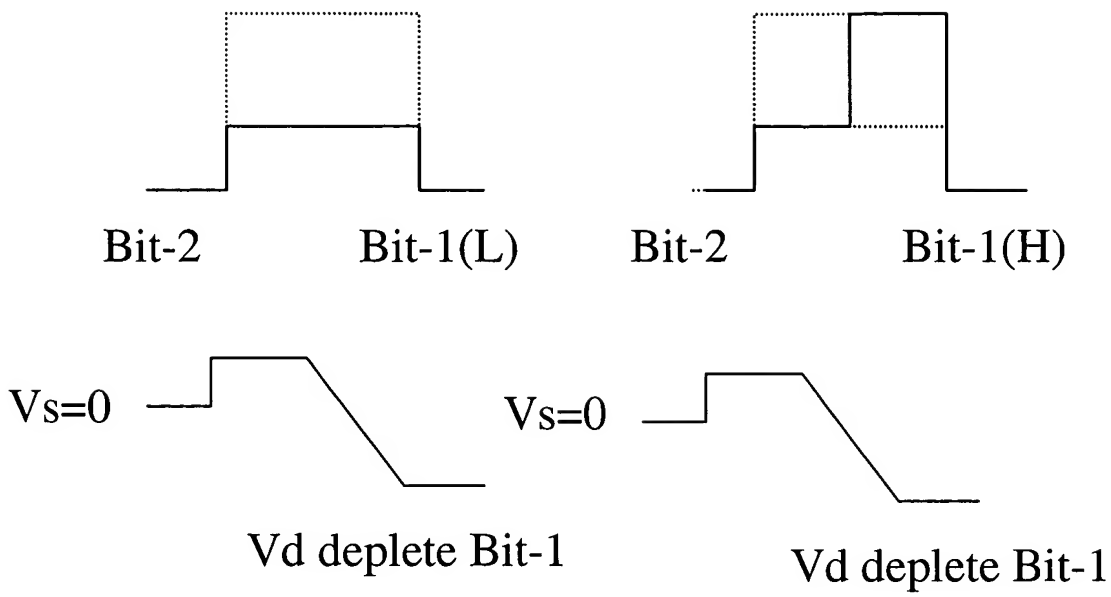



Fig. 6A Read Bit 2 (low)

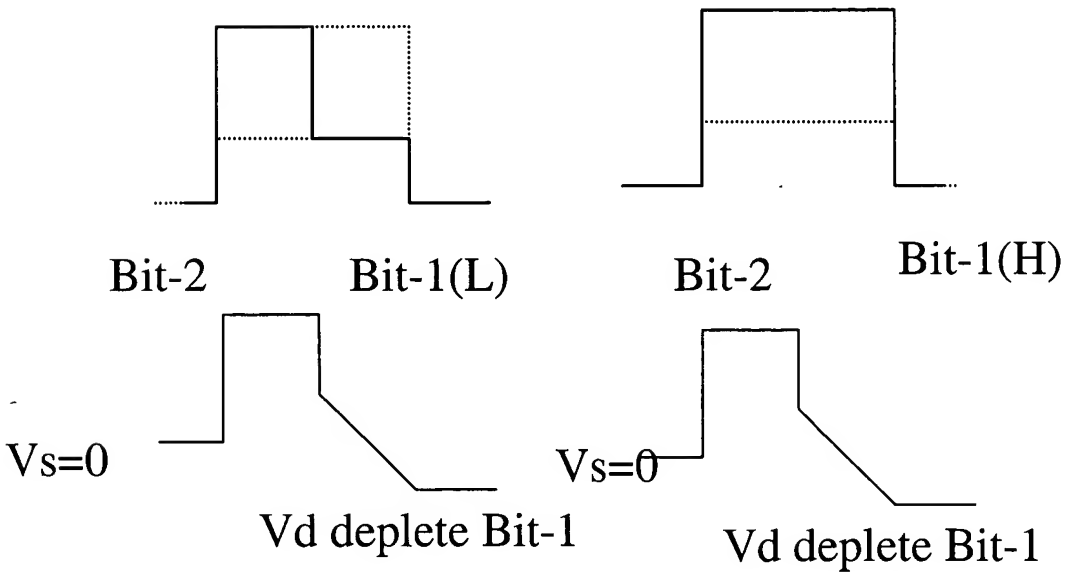



Fig. 6B Read Bit 2 (High)

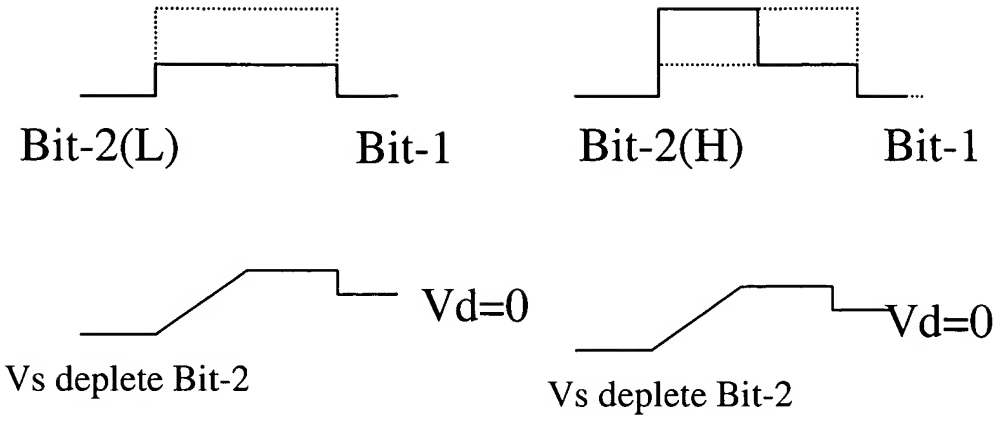



Fig. 6C Read Bit 1 (low)

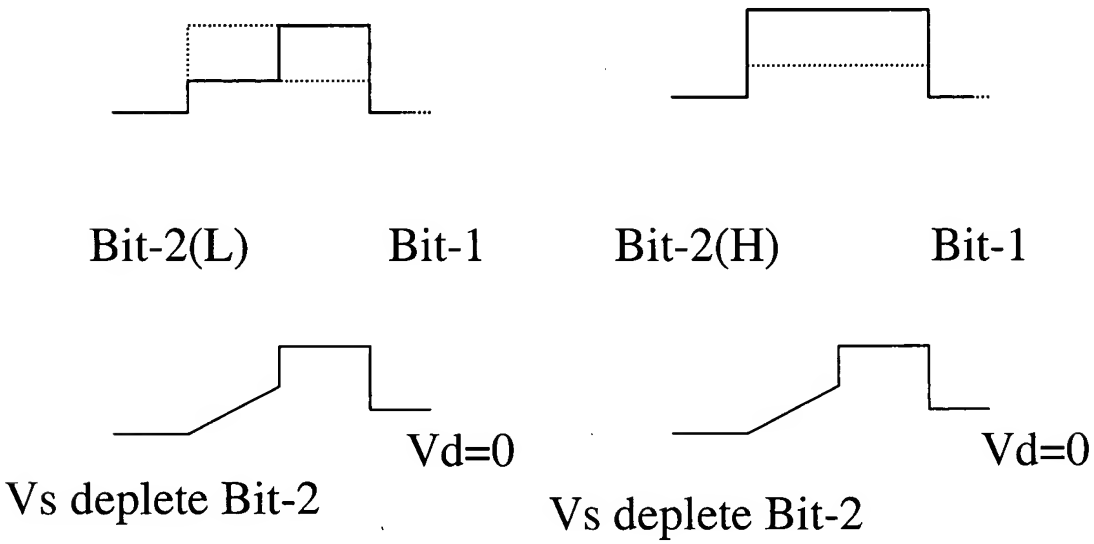



Fig. 6D Read Bit 1 (high)

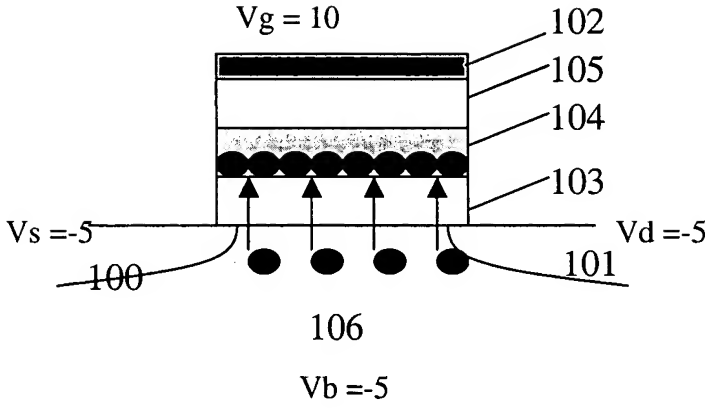

Vg = 10
102
105
104
103
Vs =-5
Vd =-5
100
101
106
Vb =-5

Fig. 7

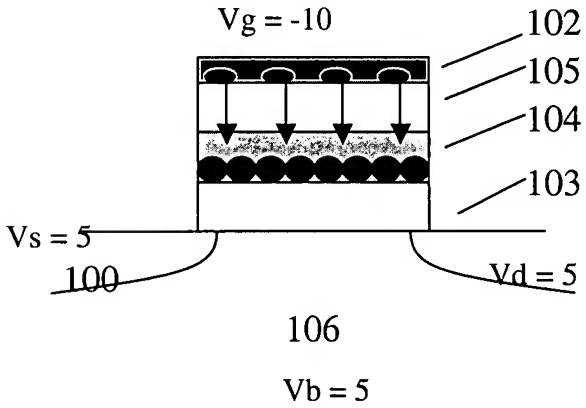

Vg = -10
102
105
104
103
Vs = 5
100
Vd = 5
106
Vb = 5

Fig. 8

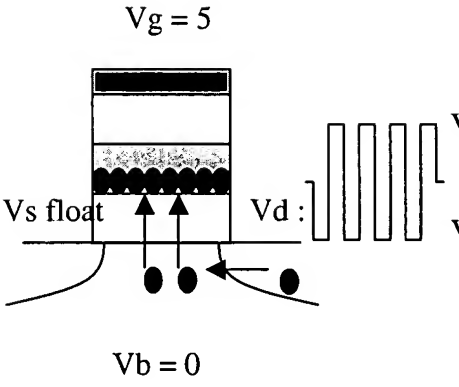



Fig. 9

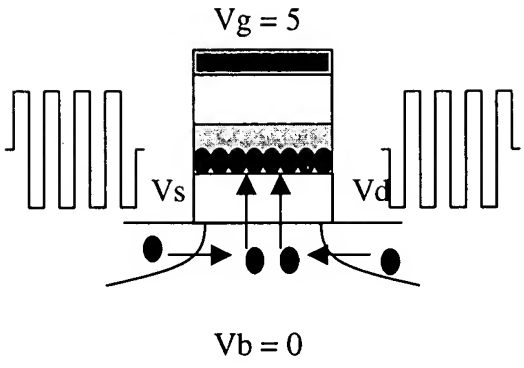



Fig. 10

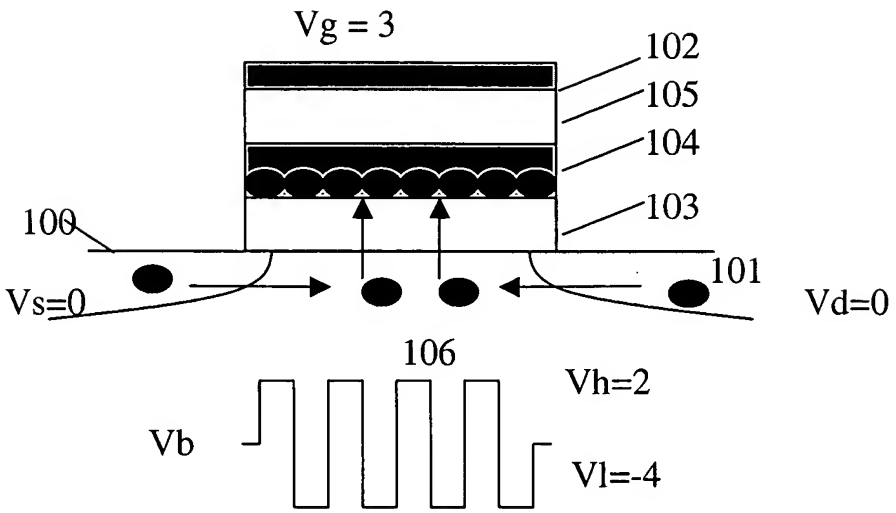



Fig. 11

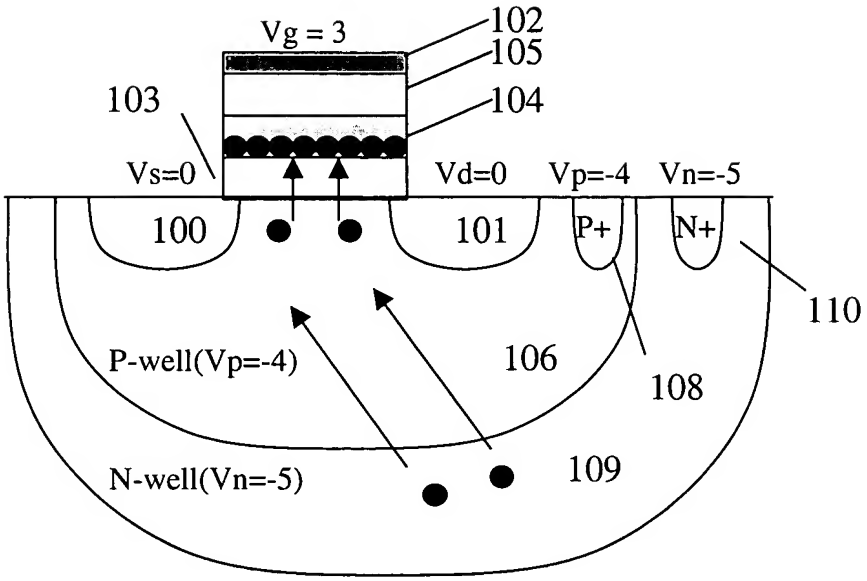

Vg = 3
102
105
104
103
Vs=0
Vd=0
Vp=-4
Vn=-5
100
101
P+
N+
110
P-well(Vp=-4)
106
108
N-well(Vn=-5)
109

Fig. 12

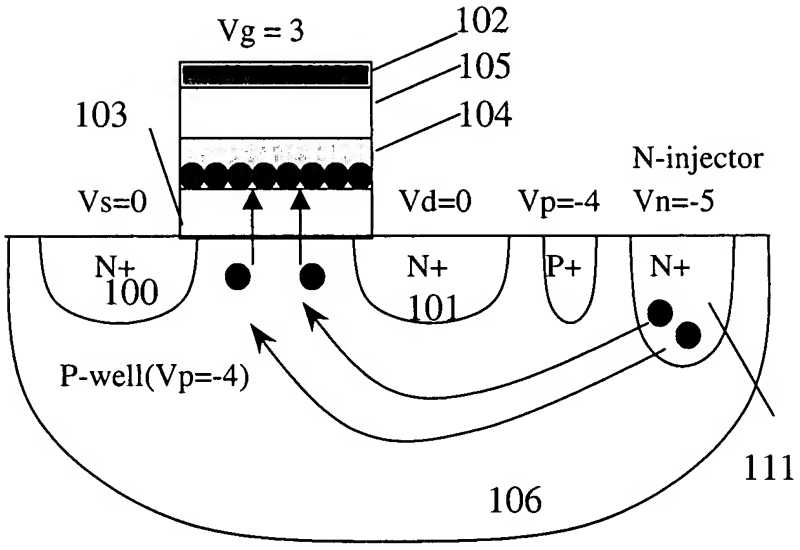

Vg = 3
102
105
104
103
N-injector
Vs=0
Vd=0
Vp=-4
Vn=-5
N+
100
N+
101
P+
N+
P-well(Vp=-4)
111
106

Fig. 13

Fig. 14

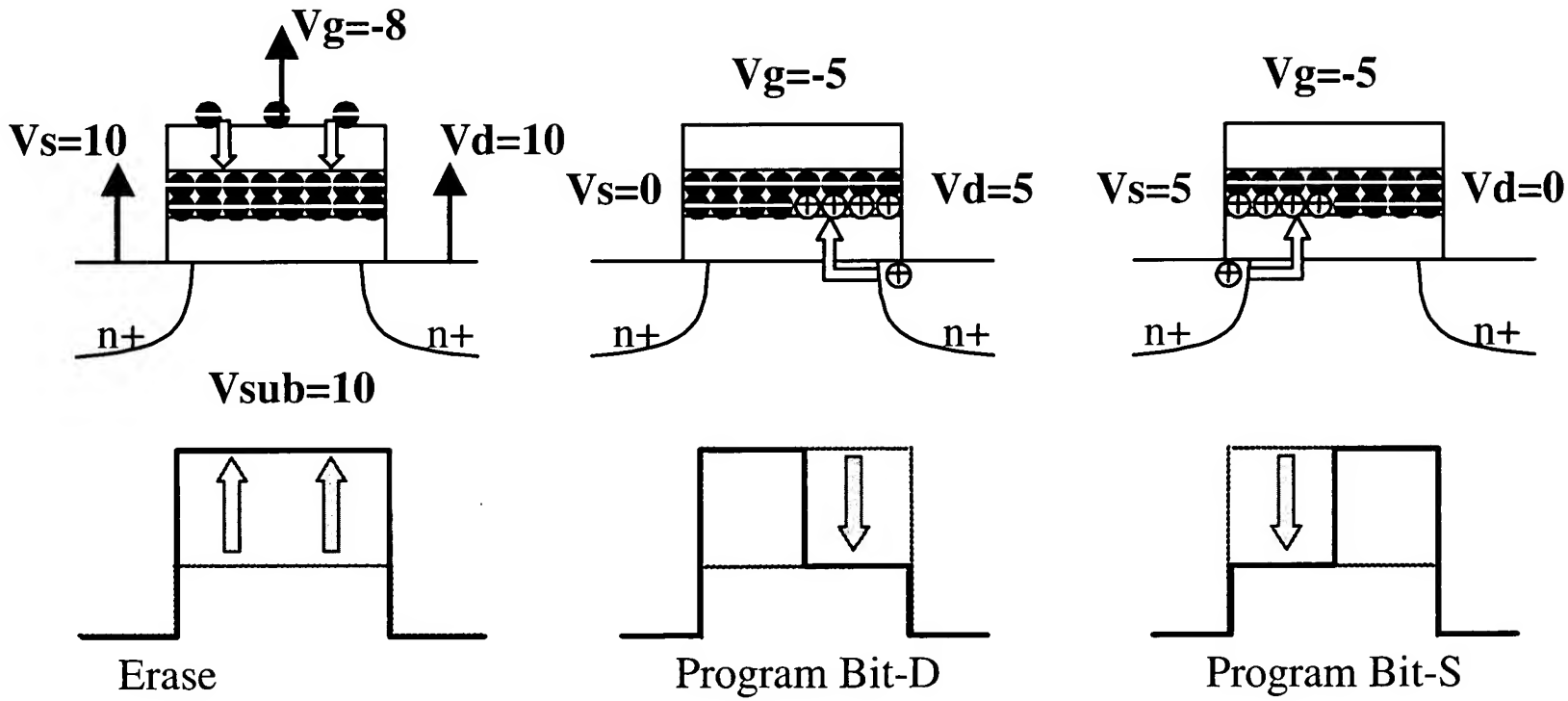
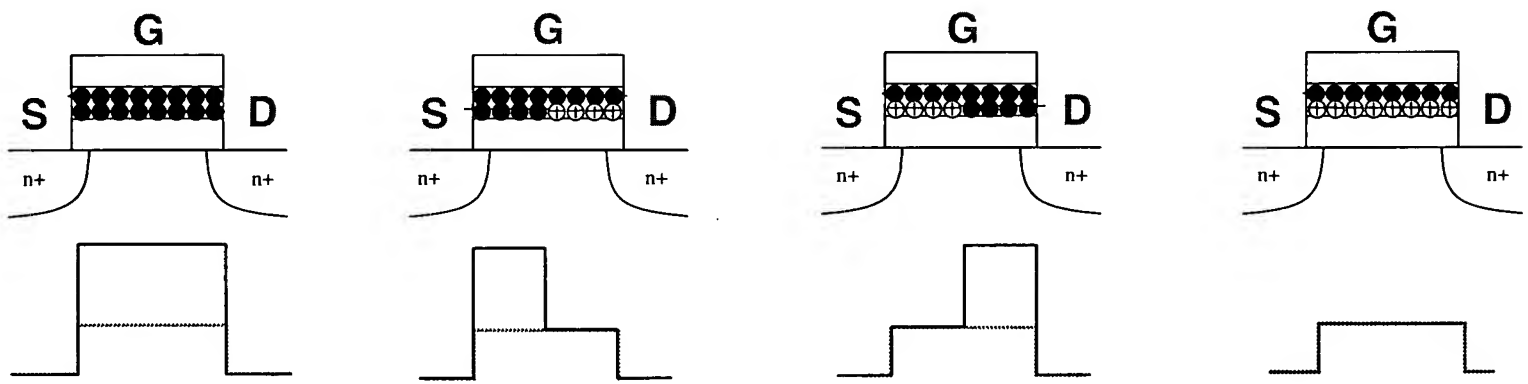
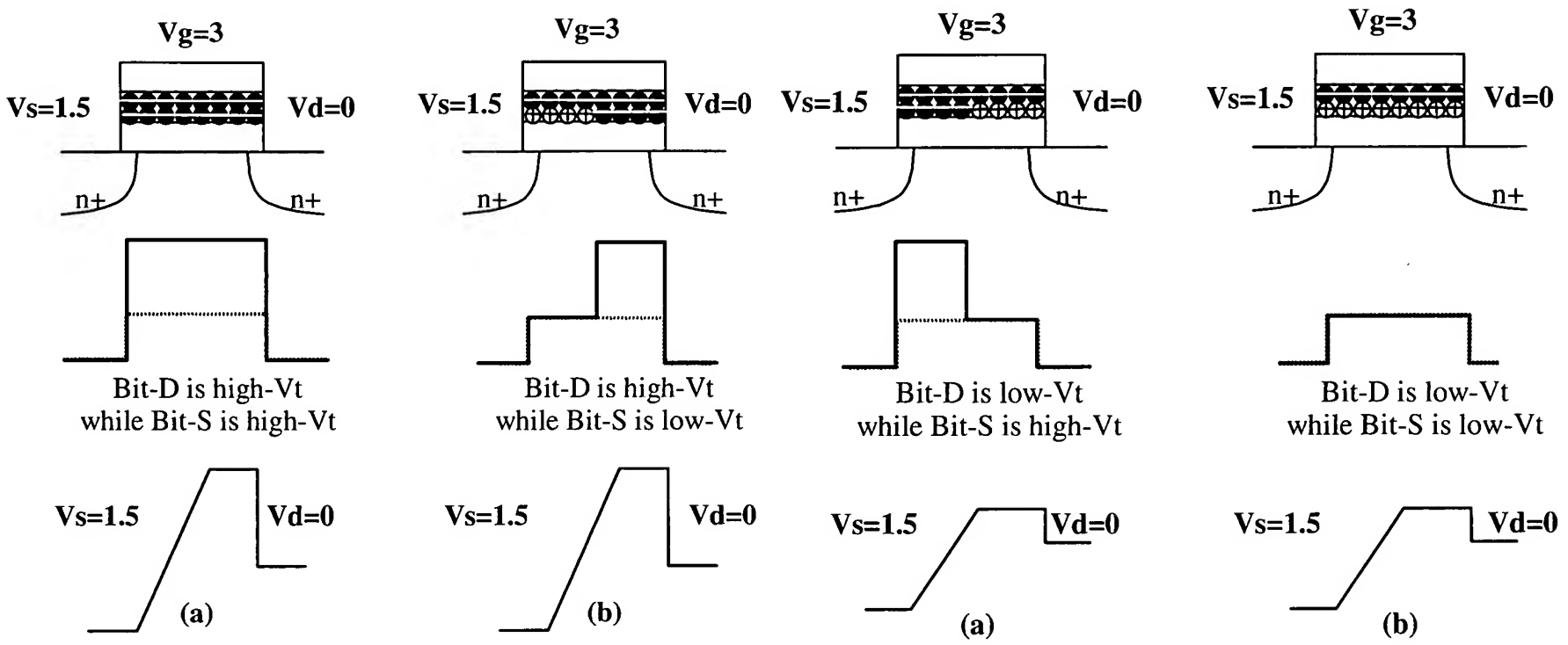

Vg=-8
Vs=10
Vd=10
n+
n+
Vsub=10
Erase
Vg=-5
Vs=0
Vd=5
n+
n+
Program Bit-D
Vg=-5
Vs=5
Vd=0
n+
n+
Program Bit-S

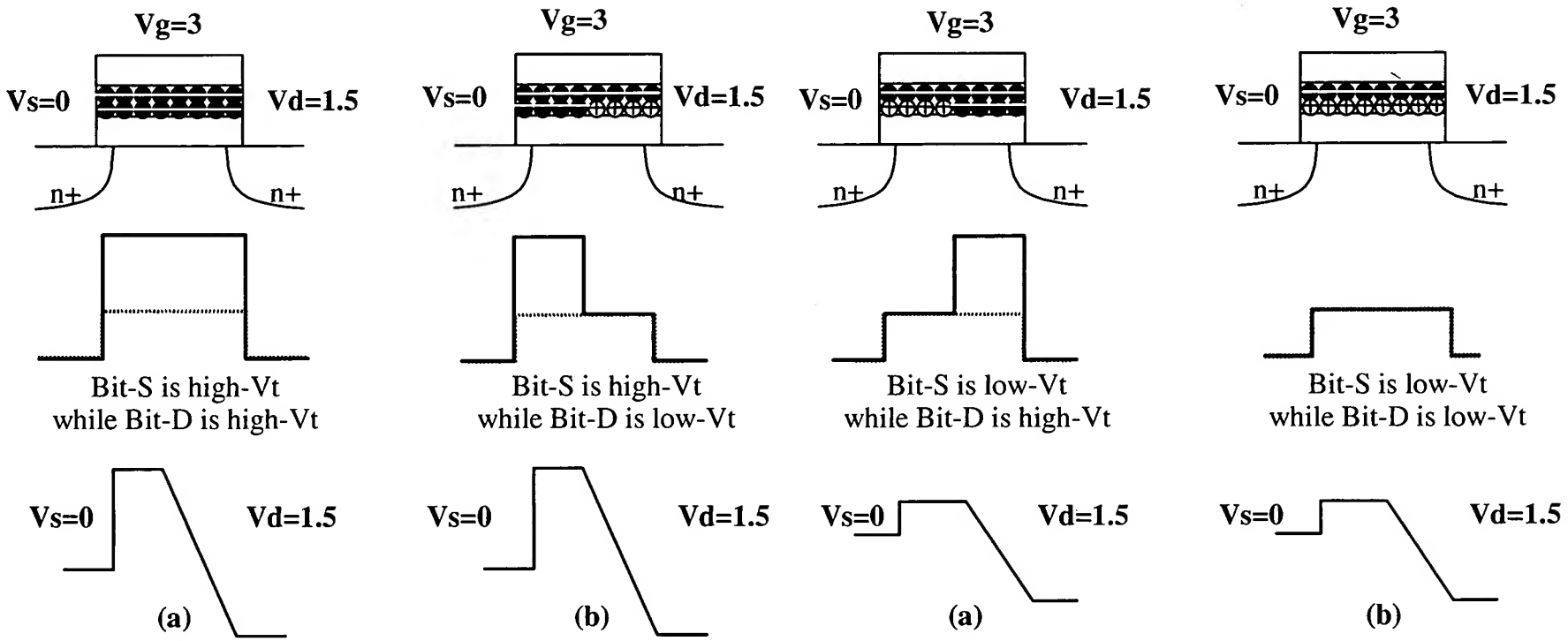
Fig. 15



# Fig. 16


Vg=3
Vs=1.5
Vd=0
n+
n+
Bit-D is high-Vt
while Bit-S is high-Vt
Vs=1.5
Vd=0
(a)
Vg=3
Vs=1.5
Vd=0
n+
n+
Bit-D is high-Vt
while Bit-S is low-Vt
Vs=1.5
Vd=0
(b)
Vg=3
Vs=1.5
Vd=0
n+
n+
Bit-D is low-Vt
while Bit-S is high-Vt
Vs=1.5
Vd=0
(a)
Vg=3
Vs=1.5
Vd=0
n+
n+
Bit-D is low-Vt
while Bit-S is low-Vt
Vs=1.5
Vd=0
(b)

# Fig. 17


Vg=3
Vs=0
Vd=1.5
n+
n+
Bit-S is high-Vt
while Bit-D is high-Vt
(a)
Vg=3
Vs=0
Vd=1.5
n+
n+
Bit-S is high-Vt
while Bit-D is low-Vt
(b)
Vg=3
Vs=0
Vd=1.5
n+
n+
Bit-S is low-Vt
while Bit-D is high-Vt
(a)
Vg=3
Vs=0
Vd=1.5
n+
n+
Bit-S is low-Vt
while Bit-D is low-Vt
(b)